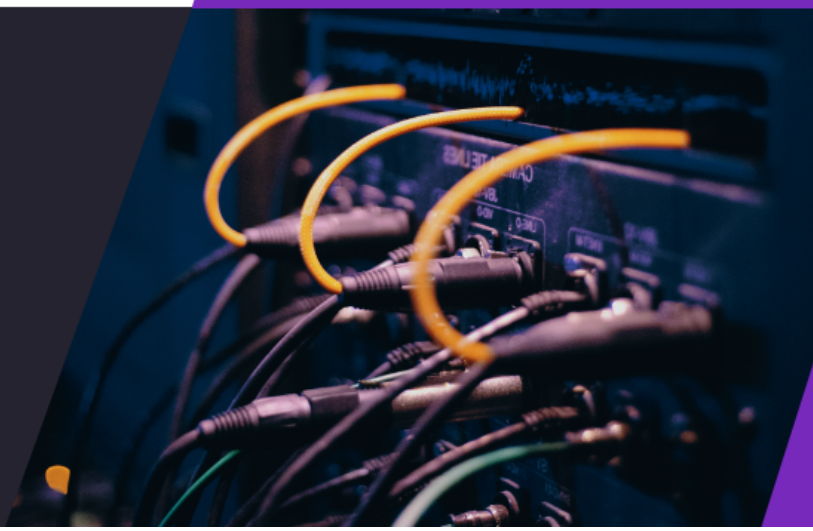
DPU QDMA Subsystem for PCIe/Ethernet



Overview

The Queue-Depth-Based Direct Memory Access (QDMA) IP is a PCI Express based DMA engine. The QDMA IP's enhanced queue depth and multi-tagging algorithm **makes it faster for high bandwidth and high volume packet count for data transfer.**

TARTH QDMA is different from other DMAs through the derived Queue set concepts of the Remote Direct memory Access (RDMA), which comes from the High Performance Computing (HPC) Interconnects. These queues can be individually configured by interface types, allowing it to function in many different modes based on how the DMA descriptors in a user logic are loaded. The user logic is dependent on a queue algorithm or technique.

We believe that processing DMA data movement should not consume excess overhead for a faster transfer.

PCI Express Interface

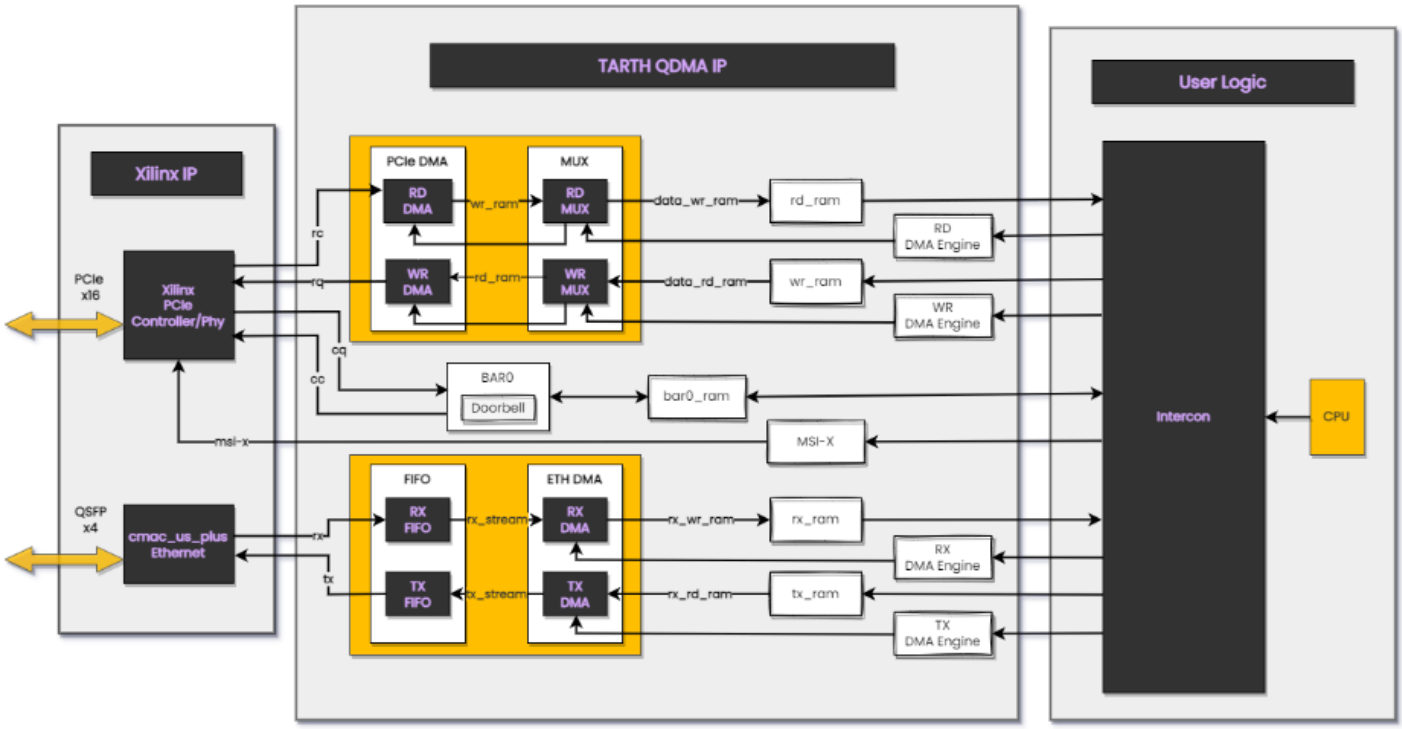
The device accesses the host processor through a x16 PCI Express v3.0 or v4.0, **capable of consuming/driving data at a rate of 32GBytes/s full-duplex.**

Each function (physical or virtual) exposes a single, prefetchable BAR that is used to post control data path commands. Both the initialization segment and the UAR pages are implemented into this BAR. This is BAR0 in the PCIe header.

Features

- Support user-define descriptor format
- Support user-define packet payload size to optimize for performance optimization
- Support for both the AXI4-Memory Mapped and AXI4-Stream interfaces per queue
- Supports Polling Mode (Status Descriptor Write Back)
- Performance: 92Gbps+ PCIe-Ethernet transfer with Xilinx FPGA
- Supports gen 3x16 link data widths up to Gen 4 PCIe
- Supports up to 512b data path
- Supports up to 2048 Queue DMA and ethernet sets
  - 2048 QDMA Write & Read Descriptor Rings
  - 2048 Ethernet TX & RX Descriptor Rings
- 2K MSI-X vectors
- Supports SR-IOV
- Ideal to replace Xilinx® LogiCORE ™ QDMA for PCI Express® (PCIe)
- Customizable to your vendor

(510) 828-3312 rcantong@tarth.net



Specifications

Components

- DPDK driver support
- Virtual I/O Device (VIRTIO) Version 1.1
- PCIe to Ethernet FPGA design
- Ethernet: 100 Gigabit
- PCIe : Gen3 x16 up to Gen4
- FPGA: Xilinx UltraScale+
- Controller to host stream interrupt moderation

Minimum Requirements

- Gen 3x16 capability requires a minimum or a 2 speed grade

Available Demos

- Demo available using poll mode driver and a Network Interface Card (NIC) bind to the poll mode driver
- Demo: Bypassing the kernel using user space

If you find yourself unsure about the TARTH QDMA, we happily **offer FREE demos** for Xilinx and VCU118 devices so that you can experiment whether or not our TARTH's subsystem is right for you.

About TARTH

With Tarth Products and IP, our services can fulfill your needs in a variety of enterprises. Whether it is for yourself or for a commercial need, our high speed connections in data, cloud, and internet can easily serve your purposes.

Our staff of experienced Network developers are available to **assist you with free evaluation** of DPU showing PCIe to Ethernet traffic running over 92Gbps using standard servers.

Why TARTH QDMA?

The TARTH QDMA IP requires **little to no work when integrating** our product to customer QDMA systems. Furthermore, TARTH QDMA IP is proven to be compatible with Mellanox versions 4 and 5.

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